CLAIMS:

1. A wafer test system comprising:

a wafer having a plurality of die to be tested,

a tester having stimulus and response outputs, and

a connection formed between said plurality of die and tester outputs.

2. A process of testing die on wafer, comprising the steps of:

contacting the die with a tester, and

inputting test stimulus and response data from the tester.

3. A process of testing die on wafer, comprising the steps of:

probing the wafer using only the number of probe contacts required for testing a single die, and

testing a plurality of die simultaneously using only said number of probe contacts.

4. A packaged IC test system comprising:

a plurality of packaged ICs to be tested,

a tester having stimulus and response outputs, and

a connection formed between said plurality of packaged ICs and tester outputs.

5. A process of testing a plurality of packaged ICs, comprising the steps of:

contacting the ICs with a tester, and

inputting test stimulus and response data from the tester.

6. An integrated circuit comprising at least one test circuit, said test circuit comprising:

a trinary gate,

a compare circuit, and

a fail flag memory.

7. A process of testing an integrated circuit comprising the steps of:

inputting test stimulus and response data to said integrated circuit, and

reading pass/fail information from the integrated circuit.

8. An integrated circuit tester comprising:

outputs for inputting stimulus data to an integrated circuit, and

outputs for inputting response data to an integrated circuit.

9. A process of using a tester to test an integrated circuit comprising the steps of:

outputting test stimulus and response data from said tester to said integrated circuit, and

inputting pass/fail information to the tester from the integrated circuit.

10. A semiconductor wafer comprising:

a plurality of identical die formed on the wafer, each die having a common set of input and output pads, and

a plurality of connections formed on the wafer, ones of said plurality of connections forming unique electrical connections between said common die input pads and unique electrical connections between said common die output pads.

11. A process of fabricating a wafer comprising the steps of:

forming a plurality of identical die on the wafer, and

forming an electrical connection between each common pad of said plurality of identical die.